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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/056,326	01/23/2002	Howard G. Sachs	021111-000300US	2891

20350 7590 09/21/2004

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EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/056,326	SACHS, HOWARD G.	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/23/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 16 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 16 recites the limitation "the second multiplexer" in lines 2 and 3. There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-10, 13, 14, and 16-19 rejected under 35 U.S.C. 102(b) as being clearly anticipated by Ellis, Jr. et al., US Patent 4,890,225.

7. Referring to claim 1, Ellis, Jr. et al. have taught a general purpose state machine comprising:

a. a first plurality of external input terminals (Figure 2, "Branch State", elements 16, 18, 26 and 22) for receiving information from an external circuit (Figure 2, elements 12, 10a-k, and 34);

b. a first multiplexer (Figure 2, element 20) having a plurality of input terminals, at least some of which are coupled to the external input terminals to receive the information therefrom (Figure 2, elements 16 and 18), the first multiplexer supplying a first output signal (Figure 2, output of element 20);

c. a programmable memory storing a plurality of words, each word having a plurality of bits (Figure 2, "Control Store"), a word from the memory being supplied in response to an address signal (Figure 2, element 32);

d. a control circuit (Figure 2, element 24 and 28) connected to receive the output signal from the first multiplexer (Figure 2, output from element 20) and connected to receive a first set of bits from a word in the programmable memory (Figure 2, element 26), the control circuit providing a signal selecting one of the words in the programmable memory (Figure 2, element 28); and

e. wherein the external circuit is connected to receive at least a second set of bits from the same word of the programmable memory as the first set of bits in response to selection of a word by the control circuit (Figure 2, element 32 is supplied to the external circuit.).

8. Referring to claim 2, Ellis, Jr. et al. have taught a general purpose state machine as in claim 1 further comprising a decoder coupled between the control circuit and the programmable memory, wherein the decoder is coupled to receive the signal from the control circuit, decode

that signal, and thereby provide the address signal to select the word to be supplied by the programmable memory (Figure 2, element 24, column 4, lines 5-27, The control store data is decoded into a control store address.).

9. Referring to claim 3, Ellis, Jr. et al. have taught a general purpose state machine as in claim 2 further comprising a register connected between the decoder and the control circuit to temporarily store the signal from the control circuit selecting one of the words in the programmable memory (Figure 2, element 10e).

10. Referring to claim 4, Ellis, Jr. et al. have taught a general purpose state machine as in claim 2 wherein the control circuit is coupled to also receive as an input signal, an address of a word previously selected (column 3, line 60-column 4, line 5).

11. Referring to claim 5, Ellis, Jr. et al. have taught a general purpose state machine as in claim 1 wherein the first set of bits received by the control circuit represents an address of a single word in the programmable memory (column 4, lines 5-9).

12. Referring to claim 6, Ellis, Jr. et al. have taught a general purpose state machine as in claim 5 wherein the signal from the control circuit selects between the address provided by the first set of bits and the address of the word previously selected (column 4, lines 20-65).

13. Referring to claim 7, Ellis, Jr. et al. have taught a general purpose state machine as in claim 5 wherein the first set of bits received by the control circuit represents addresses of two different words in the programmable memory (The first set of bits represents elements 16 and 18, the current state and the previous state.).

14. Referring to claim 8, Ellis, Jr. et al. have taught A general purpose state machine as in claim 7 wherein:

a. the control circuit is coupled to also receive as an input signal, an address of a word previously selected (column 3, line 60-column 4, line 5); and

b. the control circuit selects among the two addresses represented by the first set of bits and the address of the previously selected word (column 4, lines 20-65).

15. Referring to claim 9, Ellis, Jr. et al. have taught a general purpose state machine as in claim 1 wherein the input terminals of the first multiplexer are also connected to receive a third set of bits from the programmable memory (Figure 2, element 22).

16. Referring to claim 10, Ellis, Jr. et al. have taught a general purpose state machine as in claim 9 further comprising a second multiplexer having input terminals connected to each of the external input terminals (Figure 2, element 36), connected to the programmable memory to receive a fourth set of bits therefrom (Figure 2, "Control" and "Address"), and connected to provide an output signal to the control circuit (Figure 2, element 26).

17. Referring to claim 13, Ellis, Jr. et al. have taught a general purpose state machine as in claim 1 further comprising at least one counter coupled to at least some of the external input terminals and coupled to the first multiplexer to process information from the external circuit before it is provided to the first multiplexer (Column 3, lines 5-15).

18. Referring to claim 14, Ellis, Jr. et al. have taught a general purpose state machine as in claim 1 further comprising at least one flag circuit coupled to at least some of the external input terminals and coupled to the first multiplexer to process information from the external circuit before it is provided to the first multiplexer (Column 3, lines 5-53).

19. Referring to claim 16, Ellis, Jr. et al. have taught a general purpose state machine as in claim 14 further comprising at least one counter coupled to at least some of the external input

terminals and coupled to the second multiplexer to process information from the external circuit before it is provided to the second multiplexer (Column 3, lines 5-15).

20. Referring to claim 17, Ellis, Jr. et al. have taught a general purpose state machine as in claim 10 further comprising at least one flag circuit coupled to at least some of the external input terminals and coupled to the second multiplexer to process information from the external circuit before it is provided to the second multiplexer (Column 3, lines 5-53).

21. Referring to claim 18. Ellis, Jr. et al. have taught a general purpose state machine comprising:

a. a programmable memory storing a plurality of words, each word having a plurality of bits (Figure 2, "CONTROL STORE"), a word from the memory being supplied in response to an address signal (Figure 2, element 32);

b. a control circuit coupled to receive at least first and second address signals from a word in the programmable memory (Column 4, lines 39-4, The control circuit receives addresses from the first flow and the second flow.), and coupled to receive signals from an external circuit (column 3, line 60- column 4, line 5, The output of the multiplexer 20 is a signal from an external circuit.), control circuit selecting one of the first address or the second address in response to the signals from the external circuit (column 2, lines 18-31, column 4, lines 5-19, The first or second address is selected, i.e. not altered by the or logic, when the branching is unconditional, in response to the external signals from the external circuit.); and

c. wherein by selection of one of the address signals, the control circuit implements one of an unconditional branch operation or a two-way conditional branch operation (column 4, lines 5-19, Implements an Unconditional Branch).

22. Referring to claim 19, Ellis, Jr. et al. have taught a general purpose state machine as in claim 17 wherein:

a. the control circuit is also coupled to receive a third address signal representing a previously addressed word (column 3, line 36-column 4, line 19, The previous state represents the previously addressed word.); and

b. by selection of one of the address signals, the control circuit implements one of an unconditional branch operation, a two-way conditional branch operation, a three-way conditional branch operation, or a wait until conditional branch operation (column 4, lines 1-19).

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claim 11, 12, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellis, Jr. et al., US Patent 4,890,225.

25. Referring to claim 11, Ellis, Jr. et al. have taught a general purpose state machine as in claim 1, as described above. Ellis, Jr. et al. have not taught further comprising programmable logic coupled to at least some of the external input terminals and coupled to the first multiplexer

to process information from the external circuit before it is provided to the first multiplexer. However, Official Notice is taken that it is well known that having logic be programmable adds flexibility to a system. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Ellis, Jr. et al. further comprising programmable logic coupled to at least some of the external input terminals and coupled to the first multiplexer to process information from the external circuit before it is provided to the first multiplexer, for the desirable purpose of increasing the overall flexibility of the system.

26. Referring to claim 12, Ellis, Jr. et al. have taught a general purpose state machine as in claim 11 wherein the programmable logic comprises: a first plurality of multiplexers connected in parallel to a plurality of external input terminals to provide a corresponding first plurality of output lines, each of the first plurality of multiplexers having a plurality of input terminals, each one of which is coupled to one of a first potential source and a second potential source (Figure 2, elements 20 and 36). Ellis, Jr. et al. have not specifically taught a second plurality of multiplexers also connected in parallel to the plurality of external input terminals to provide a corresponding second plurality of output lines, each of the second plurality of multiplexers having a plurality of input terminals, each one of which is coupled to one of the first potential source and the second potential source. However, duplicating parts for multiple effect has been held to not yield a patentable difference over the prior art, see *In re Harza*, 274 F.2d 669, 671, 124 USPQ 378, 380 (CCPA 1960). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Ellis, Jr. et al. include a second plurality of multiplexers also connected in parallel to the plurality of external input terminals to provide a corresponding second plurality of output lines, each of the second plurality

of multiplexers having a plurality of input terminals, each one of which is coupled to one of the first potential source and the second potential source, because the duplication of parts, i.e. the plurality of multiplexers, for a multiple effect is not a patentable difference.

27. Referring to claim 15, Ellis, Jr. et al. have taught a general purpose state machine as in claim 10, as described above. Ellis, Jr. et al. have not specifically taught further comprising programmable logic coupled to at least some of the external input terminals and coupled to the second multiplexer to process information from the external circuit before it is provided to the second multiplexer. However, Official Notice is taken that it is well known that having logic be programmable adds flexibility to a system. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Ellis, Jr. et al. further comprising programmable logic coupled to at least some of the external input terminals and coupled to the second multiplexer to process information from the external circuit before it is provided to the second multiplexer, for the desirable purpose of increasing the overall flexibility of the system.

Conclusion

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 8-4:30.

29. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

30. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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